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UTILITY PATENT APPLICATION TRANSMITTAL (Only for new nonprovisional applications under 37 CFR 1.53(b))		
	Attorney Docket No.	**NS-3877-2D US**
	First Named Inventor or Application Identifier	Mostafazadeh et al.
	Title	"Lead Frame Chip Scale Package"
	Express Mail Label No.	**EL 487 695 812 US**

APPLICATION ELEMENTS
See MPEP chapter 600 concerning utility patent application contents

ADDRESS TO: Assistant Commissioner for Patents, Box Patent Application, Washington, D.C. 20231

1. ☒ Fee Transmittal Form - ***see page 2 of this form.*** (Submit an original, and a duplicate for fee processing)
2. Application:
   - ☒ Specification: (preferred arrangement set forth below)
     Descriptive title of the Invention,
     Cross References to Related Applications,
     Reference to Microfiche Appendix,
     Background of the Invention,
     Brief Summary of the Invention,
     Brief Description of the Drawings, and
     Detailed Description (all totaling 7 pages)
     Appendix(ces) ___, ___, & ___ (___pages)
   - ☒ Claim(s) 2 pages
   - ☒ Abstract of the Disclosure 1 page
3. ☒ Drawing(s) (35 USC 113) [Total Sheets 7]
4. Oath or Declaration ☐ unsigned [Total Pages ___]
   - a. ☐ Newly executed (original or copy)
   - b. ☒ Copy from prior application (37 CFR §1.63(d)) (for continuation/divisional with Box 17 completed)
   - c. ☐ DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1 63(d)(2) and 1 33(b)
5. ☒ Incorporation By Reference (useable if Box 4b is checked) The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
6. ☐ Microfiche Computer Program Appendix consisting of ___ pages of microfiche containing ___ frames on each page in accompanying envelope.
7. Nucleotide and/or Amino Acid Sequence Submission (if applicable, all necessary)
   - a. ☐ Computer Readable Copy
   - b. ☐ Paper Copy (identical to computer copy)
   - c. ☐ Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. ☒ Assignment Papers (cover sheet & documents) 3 pages
9. ☐ ~~37 CFR §3.73(b) Statement~~ ☒ ~~Power of Attorney~~ (combined when there is an Assignee) with Patent Declaration above.)
10. ☐ English Translation Document (if applicable)
11. ☐ Information Disclosure Statement (IDS) & ☐ PTO-1449 ☐ ___Copies of IDS Citations/References
12. ☒ Preliminary Amendment 3 pages
13. ☒ Return Receipt Postcard (MPEP 503) (should be specifically itemized)
14. Small Entity Status
    - ☐ Small Entity Statement Enclosed ___ pages
    - ☐ Statement filed in prior application; and status still proper and desired
    - ☐ Is no longer claimed.
15. ☐ Certified Copy of Priority Document(s) (if foreign priority is claimed)
16. ☒ Other:
    - ☐ Copy of Petition for Extension of Time filed in parent appln.;
    - ☐

17. If a CONTINUING APPLICATION, check appropriate box and supply the requisite information and a preliminary amendment:
    ☐ Continuation ☒ Divisional of prior application No. 09/054,422
    Filed on April 2, 1998, entitled: "Lead Frame Chip Scale Package".
    PRIOR APPLICATION INFORMATION: *Examiner* **Clark, S.** Group *Art Unit* **2815**

18. CORRESPONDENCE ADDRESS

☐ Customer Number or Bar Code Label or ☒ Correspondence address below

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Attorneys for Applicant	**Skjerven Morrill MacPherson LLP**				
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09/399,585

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19. Fee calculations.

CLAIMS (Number Filed)	(1) FOR	(2)		(3) NUMBER EXTRA		(4) RATE		(5) CALCULATIONS
7	TOTAL CLAIMS (37 CFR 1.16(c))	-20	=	0	x	$18	=	$ 0.00
1	INDEPENDENT CLAIMS (37 CFR 1.16(b))	-3	=	0	x	$78	=	$ 0.00
☐	MULTIPLE DEPENDENT CLAIMS (if applicable) (37 CFR 1.18(d))				+	$260.00	=	
				BASIC FEE (37 CFR 1.16(a))			=	$ 690.00
				Total of above Calculations			=	$ 690.00
	Reduction by 50% for filing by small entity (Note 31 CFR 1.9, 1.27, 1.28).						=	
				TOTAL			=	$ 690.00

20. FEES: The Commissioner is hereby authorized to credit overpayments or charge the following fees to Deposit Account No. **19-2386**:
   a. ☒ Fees required under 37 CFR 1.16. (U.S. Application Filing Fees)
   b. ☒ Fees required under 37 CFR 1.17. (Conditional Extension of Time Fees)
   c. ☐ Fees required under 37 CFR 1.18. (Patent Issue Fees)

21. ☐

NOTE: The prior application's correspondence address will carry over to this UPA UNLESS a new correspondence address is provided below.

22. NEW CORRESPONDENCE ADDRESS

Customer Number or Bar Code Label _____ New correspondence address below _____

NAME					
ADDRESS					
CITY		STATE		ZIP CODE	
COUNTRY		TELEPHONE		FAX	

23. SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

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Date:		
Name	Edward C. Kwok	Reg. No. 33,938
Signature		
Express Mail Label No.	**EL 487 695 812 US**	

655236 v1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Mostafazadeh, Shahram; Smith, Joseph O.		
Assignee:	National Semiconductor Corp.		
Title:	Lead Frame Chip Scale Package		
Serial No.:	Unassigned	Filing Date:	Herewith
Examiner:	Unknown	Group Art Unit:	Unknown
Docket No.:	NS-3877-2D US		

San Jose, California
July 25, 2000

BOX PATENT APPLICATION
COMMISSIONER FOR PATENTS
Washington, D. C. 20231

PRELIMINARY AMENDMENT

Dear Sir:

Please amend the above-referenced patent application as follows:

IN THE CLAIMS

Please cancel Claims 1-10.

Please add Claims 11-17 as follows:

11. An integrated circuit package for accommodating a semiconductor die, comprising:

a lead frame comprising (a) a die attach pad supporting said semiconductor die on an upper surface of said die attach pad, and (b) conductive leads positioned around an outer periphery of said die attach pad, wherein each of said conductive leads having a lower surface that is substantially coplanar with said lower surface of said die attach

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pad, said upper and lower surfaces of said die attach pad being located on opposite sides of said die attach pad;

a plurality of bond wires each coupling one of said conductive leads to a corresponding bonding pad on said semiconductor die; and

a plastic encapsulation enclosing said semiconductor die, said bond wires and said lead frame, exposing at a lower surface of said plastic encapsulation said lower surface of said die attach pad and said lower surfaces of said conductive leads.

12. An integrated circuit package as in Claim 11, further comprising a solder ball attached to each of said exposed lower surface of said conductive leads.

13. An integrated circuit package as in Claim 11, further comprising an adhesive pad removably attached to said integrated circuit package, covering said lower surface of said die attach pad and said lower surfaces of said conductive leads.

14. An integrated circuit package as in Claim 13, wherein said integrated circuit package is one of a plurality of integrated circuit packages fabricated simultaneously from said lead frame, said lead frame comprising an array of die attach pads and conductive leads, and wherein said adhesive pad supports die attach pads and said conductive leads prior to singulation of said plurality of integrated circuit packages.

15. An integrated circuit package as in Claim 14, wherein said lead frame is fabricated on a metal panel.

16. An integrated circuit package as in Claim 15, further comprising an encapsulant dam provided to enclose said array of die attach pads and conductive leads.

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17. An integrated circuit package as in Claim 14, wherein said array of die attach pads and conductive dies is being arranged in a regular pattern so as to allow singulation of said integrated circuit packages by sawing through said plastic encapsulation and said conductive leads at predetermined positions.

REMARKS

Claims 1-10 are canceled. Claims 11-17 are newly presented to more particularly point out and distinctly claim Applicants' invention.

If the Examiner has any questions regarding the above, the Examiner is respectfully requested to telephone the undersigned Attorney for Applicants at 408-453-9200.

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Respectfully submitted,

Edward C. Kwok
Attorney for Applicants
Reg. No. 33,938

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LEAD FRAME CHIP SCALE PACKAGE

Shahram Mostafazadeh
Joseph O. Smith

BACKGROUND INFORMATION

Field of the Invention

The present invention relates to integrated circuit packages, and more specifically, to the production of a chip scale integrated circuit package using a lead frame.

Related Art

An integrated circuit (IC) package encapsulates an IC chip, or die, in a protective casing and also provides power and signal distribution between the IC chip and an external printed circuit board (PCB). A common IC package uses a metal lead frame to provide the electrical paths for that distribution. For production purposes, a lead frame panel 110 made up of multiple lead frames 120 is etched or stamped from a thin sheet of metal, as shown in Fig. 1a. An IC chip 130 is then mounted and wire bonded to each lead frame 120, as shown in Fig. 1b. Wire bonding is typically performed using fine gold wires 140. Each IC chip 130 is then encapsulated in a protective casing 160, which can be produced by installing a preformed plastic or ceramic housing around each IC chip 130, or by dispensing and molding a layer of encapsulant material over all IC chips 130. Next, lead frames 120 are cut apart, or singulated, and multiple electrical interconnections are attached to the lead frame in order to produce individual IC packages 190, as shown in Fig. 1c. The electrical interconnections provide the electrical interface between IC package 190 and the external PCB, and can take a variety of forms. Fig. 1c

depicts a lead frame ball grid array (BGA) IC package in which electrical interconnections are provided by solder balls 150 mounted on the bottom surface of lead frame 120. Other types of electrical interconnections can be seen in Fig. 1d, which shows examples of common IC packages using lead frames, including a small outline package (SOP) 191, a pin-through-hole (PTH) package 192, and a plastic leaded chip carrier (PLCC) 193.

The use of a lead frame provides an inexpensive means for IC package manufacturing. Etching or stamping a sheet of thin metal to produce the desired lead frame patterns is a well-known manufacturing process, and is conducive to high-volume, low-cost production. In addition, the lead frame panel provides a support framework for the IC chips during IC package assembly. However, as IC chip device densities increase and IC package sizes decrease, the geometries used in the electrical communication paths between the IC chip and the PCB decrease. For example, a chip scale package requires that the protective casing be no more than 20% larger than the IC chip. As a result, the area available for the electrical paths provided by the lead frame is significantly reduced, demanding much finer lead frame patterns. In order to construct that finer geometry, the lead frame thickness must be reduced to a point where the lead frame panel rigidity would no longer be sufficient to provide the necessary support during the IC package assembly process. Also, the fragile lead frame patterns would be more susceptible to damage during the manufacturing process. As a result, chip scale IC packages must use more costly techniques such as tape automated bonding (TAB) or printed substrate backing.

Accordingly, it is desirable to provide an IC packaging method that allows the use of a lead frame in a chip scale package.

SUMMARY OF THE INVENTION

The present invention provides a method for producing chip scale IC packages using lead frames. A temporary support fixture provides support and stability to a thin lead frame panel having the fine geometries required for higher-density IC chip interfaces. An embodiment of the support fixture includes an adhesive pad made of one-sided sticky tape mounted to a rigid frame made of stainless steel, the rigid frame maintaining the adhesive pad in a fixed configuration providing a stable flat surface for support of the lead frame panel. Alternatively, the rigid frame and adhesive pad can be made of any materials compatible with the IC package manufacturing process and capable of supporting the lead frame panel through the manufacturing process. The adhesive pad can also be patterned to ease the manufacturing process. The rigid frame can include positioning features to assist in the alignment of the lead frame and adhesive pad. If encapsulant material is to be dispensed over the lead frame panel, a containment dam can be formed around the lead frame after it is installed on the adhesive pad, to provide a boundary for encapsulant material flow.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1a shows a representation of a typical lead frame panel;

Fig. 1b shows a lead frame panel populated with IC chips;

Fig. 1c shows a single leadframe BGA IC package;

Fig. 1d shows examples of common IC packages;

Fig. 2a shows an embodiment of a rigid support fixture;

Fig. 2b shows a lead frame panel mounted on an embodiment of a support fixture;

Figs. 3a and 3b show a flow diagram of a manufacturing process using a temporary support fixture.

Use of the same reference number in different figures indicates similar or like elements.

DETAILED DESCRIPTION

The present invention employs a rigid support fixture during the manufacturing process to enable the use of lead frames in chip scale IC packages. An embodiment of a support fixture 200 includes a rigid frame 210 and an adhesive pad 220, as shown in the exploded isometric diagram of Fig. 2a. Because pad 220 is affixed along its border to frame 210, it maintains sufficient tension to provide a stable supporting surface for a lead frame panel 110. By making pad 220 out of a thin, flexible, and electrically non-conductive material, it provides a support structure that will not interfere with the conventional manufacturing processes used in IC package assembly. The size of the interior opening of frame 210 is large enough to allow lead frame panel 110 to be fully supported by pad 220. Multiple IC chips 130 are then installed and wire bonded on lead frame panel 110, as shown in Fig. 2b. Subsequent encapsulation of IC chips 130 in protective casings proceeds as in conventional lead frame processing. If a molded protective casing is to be applied, an encapsulant dam 240 can be constructed around the perimeter of lead frame panel 110. Dam 240 can be made of any substantially rigid substance, including premolded plastic, epoxy, or tape,

and serves to prevent flow of encapsulant material beyond the boundaries of lead frame panel 110. Alternatively, containing measures for encapsulant material could be incorporated into the dispensing mechanism. Once encapsulation is complete, support fixture 200 can be removed, either before or after singulation.

The embodiment of the present invention shown in Figs. 2a and 2b can be constructed from common and readily available materials. Pad 220 can be made from a 3M or Nitto-brand sticky tape used in conventional wafer saw operations. Likewise, a stainless steel ring of the type used in conventional wafer saw operations can be employed for frame 210. However, both pad 220 and frame 210 can be implemented in many different ways as well. For example, frame 210 can be constructed from any rigid material compatible with the IC package assembly process, such as copper, aluminum, or even non-metals such as ceramic or plastic. Also, while depicted as a thin circular element, frame 210 can also take a variety of configurations depending on handling, interface, and user requirements. For instance, frame 210 can include positioning features to ensure consistent alignment for lead frame panel 110 and adhesive pad 220. A circular outline for frame 210 provides compatibility with conventional handling requirements for IC production, but is not a required aspect of the present invention.

Similarly, numerous implementations of adhesive pad 220 are possible. Any material compatible with the IC package assembly process and capable of providing the necessary support to the lead frame panel and IC chips can be used. The sticky tape mentioned previously is a convenient choice due to widespread current usage and availability. The use of one-sided sticky tape enables pad 220 to be applied to the bottom

surface of frame 210 and provide an adhesive surface for mounting of lead frame panel 110, without requiring additional attachment materials or components. Pad 220 can also be patterned by removing selected portions in order to facilitate subsequent assembly operations such as electrical interconnection formation. Removal of pad 220 once packaging is complete can be performed in various ways, depending on the nature of the adhesive material used. A light adhesive material may allow pad 220 to simply be peeled away from frame 110. An alternative bonding agent requires exposure to UV light before removal of pad 220 can take place.

Figs. 3a and 3b show a graphical flow chart illustrating a method for manufacturing a lead frame BGA package using an embodiment of the present invention. The manufacturing process is described in conjunction with the elements described in Figs. 2a-2c. In a step 310 in Fig. 3a, adhesive pad 220 is applied to rigid frame 210 to create support fixture 200. Lead frame panel 110 is then mounted on pad 220 in a step 320. An optional step 330 allows encapsulant dam 240 to be applied around the border of lead frame panel 110 if subsequent encapsulant material dispensing is to be performed. Next, an IC chip 130 is mounted and wire bonded onto each of the lead frames 120 of lead frame panel 110. Continuing the process in Fig. 3b, a step 350 involves dispensing a portion of encapsulant material 170 into the area defined by dam 240 to cover IC chips 130, and then curing material 170 to a desired hardness. In a step 360, pad 220 is removed from lead frame panel 110. Next, in a step 370, a wafer saw operation is performed to singulate lead frame panel 110 into individual IC packages. The singulation process converts the layer of hardened encapsulant material 170 into individual protective casings 160. Finally, in a step 380, solder balls 150 are applied to

desired electrical interconnection locations to complete lead frame BGA IC package 190.

In this manner a lead frame BGA IC package can be produced using a temporary support structure. This enables the production of IC packages using lead frames that would otherwise be too fragile to withstand conventional manufacturing processes. It should be noted that while particular embodiments of the present invention have been shown and described, it will be apparent to those skilled in the art that many modifications and variations thereto are possible, all of which fall within the true spirit and scope of the invention. For example, the wafer saw operation of step 370 can be performed prior to removal of support fixture 200 from lead frame panel 110. Also, solder balls 150 could be applied to lead frames 120 in step 370 prior to singulation. Alternatively, appropriately located openings in adhesive pad 220 would allow solder balls 150 to be applied without removing pad 220. Certain lead frame designs may even allow patterning of pad 220 such that removal is unnecessary. Finally, while the present invention has been described with reference to chip scale IC package manufacturing, it can be applied to any IC package manufacturing process involving lead frames, including non-chip scale and non-BGA IC packages such as SOP's, PLCC's, and PTH packages.

CLAIMS

We Claim:

1. A method for IC package production comprising the steps of:

creating a plurality of lead frames joined into a single lead frame panel;

attaching said lead frame panel to a removable support fixture;

installing a plurality of IC chips onto said plurality of lead frames;

encapsulating each of said plurality of IC chips in a protective housing; and

singulating said plurality of lead frames.

2. The method of Claim 1 wherein said singulating step comprises the steps of:

removing said support fixture from said plurality of lead frames;

cutting said lead frame panel into said plurality of lead frames; and

creating a plurality of electrical interconnections on said plurality of lead frames.

3. The method of Claim 1 wherein said attaching step comprises the steps of:

mounting an adhesive pad on a rigid frame such that said adhesive pad forms a taut surface across an interior opening of said rigid frame, said interior opening being larger than the border of said lead frame panel; and

mounting said lead frame panel on said adhesive pad such that said lead frame panel is completely within said interior opening.

4. The method of Claim 3 wherein said adhesive pad is constructed of single-sided sticky tape and is affixed around its border to said rigid frame.

5. A fixture for providing temporary support to a lead frame during an IC package manufacturing process comprising an adhesive pad attached to a rigid frame such that said adhesive pad is held in tension by said rigid frame to provide a stable support surface for said lead frame.

6. The fixture of Claim 5 wherein said adhesive pad is constructed of single-sided sticky tape.

7. The fixture of Claim 6 wherein said rigid frame comprises a stainless steel ring having an opening of diameter larger than said lead frame.

8. The fixture of Claim 5 wherein said rigid frame includes a set of positioning features for positioning and aligning said lead frame and said adhesive pad with respect to said rigid frame.

9. The fixture of Claim 5 wherein said adhesive pad is patterned to facilitate a subsequent manufacturing step.

10. A method for applying a layer of an encapsulant material over a lead frame panel populated with a plurality of IC chips comprising the step of creating an encapsulant dam around the perimeter of said lead frame panel, said encapsulant dam being a substantially rigid barrier capable of blocking the flow of said encapsulant material.

LEAD FRAME CHIP SCALE PACKAGE

Shahram Mostafazadeh
Joseph O. Smith

ABSTRACT

A method for producing chip scale IC packages includes the step of mounting a lead frame panel on a temporary support fixture in order to provide support and protection during the manufacturing process. An embodiment of the temporary support fixture includes a sheet of sticky tape secured to a rigid frame. The rigid frame maintains tension in the sheet of sticky tape to provide a stable surface to which the lead frame panel can be affixed. Installation of IC chips and encapsulation in protective casings is performed as in conventional IC package manufacturing. If encapsulant material is to be dispensed over the IC chips, an encapsulant dam can be formed around the lead frame panel to contain the flow of encapsulant material. The temporary support fixture can be used in any IC package manufacturing process in which lead frames require supplemental support.

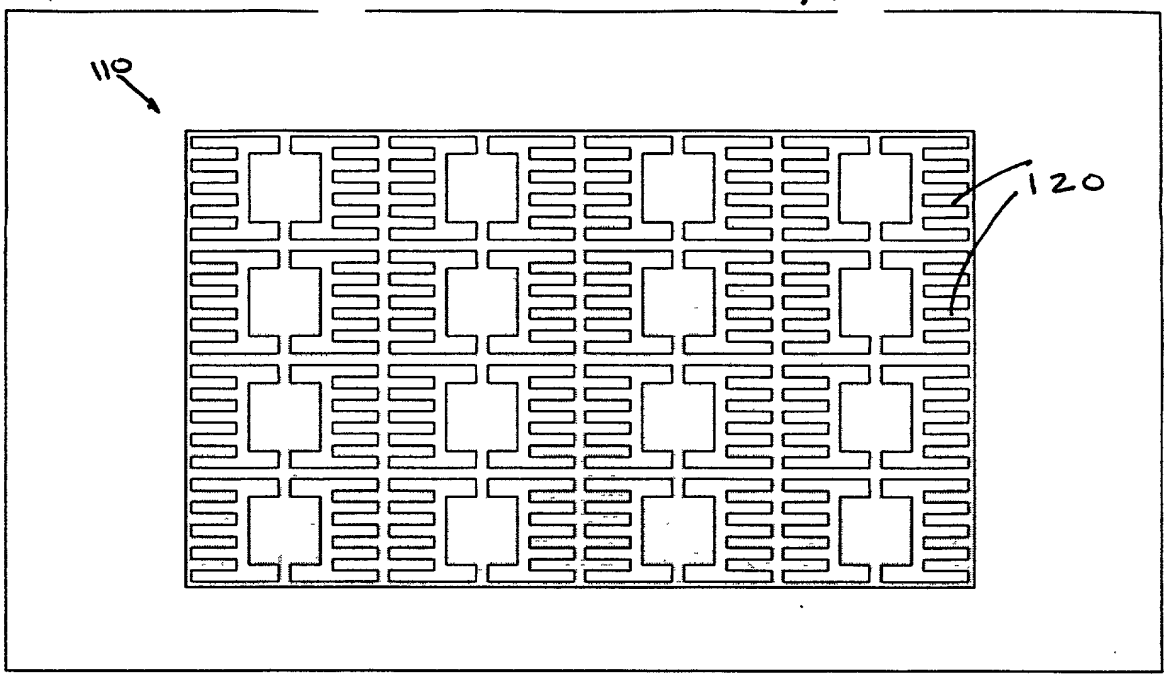

Fig. 1a: Embodiment of a Lead Frame Panel

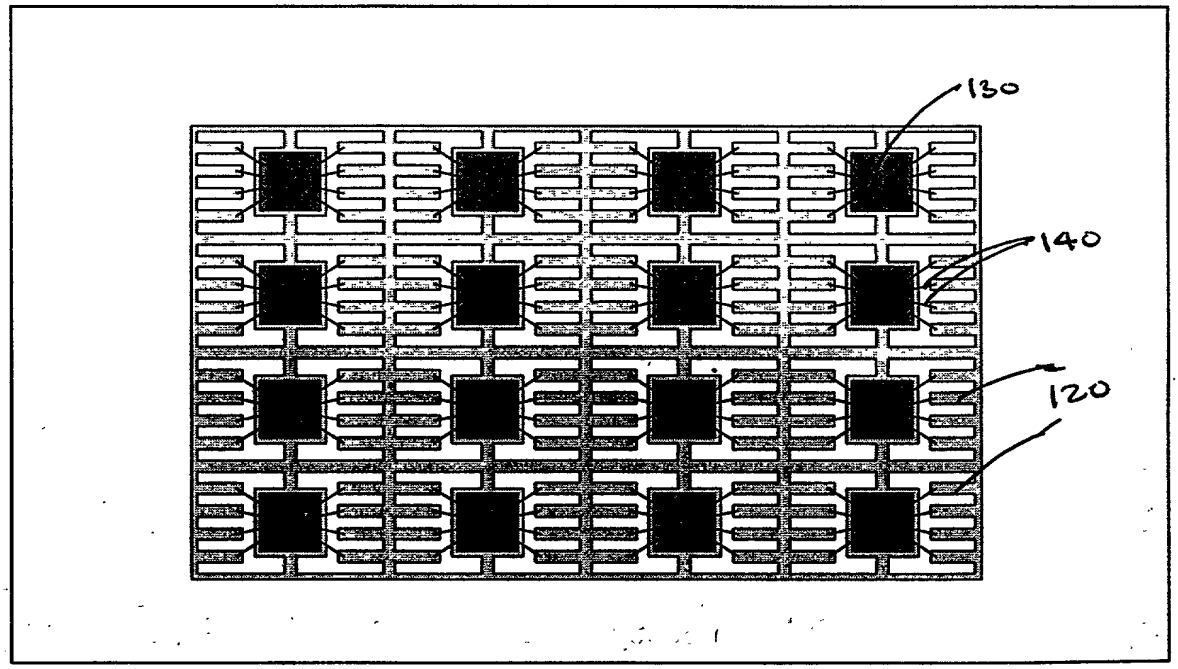

Fig. 1b: Lead Frame with IC Chips Attached

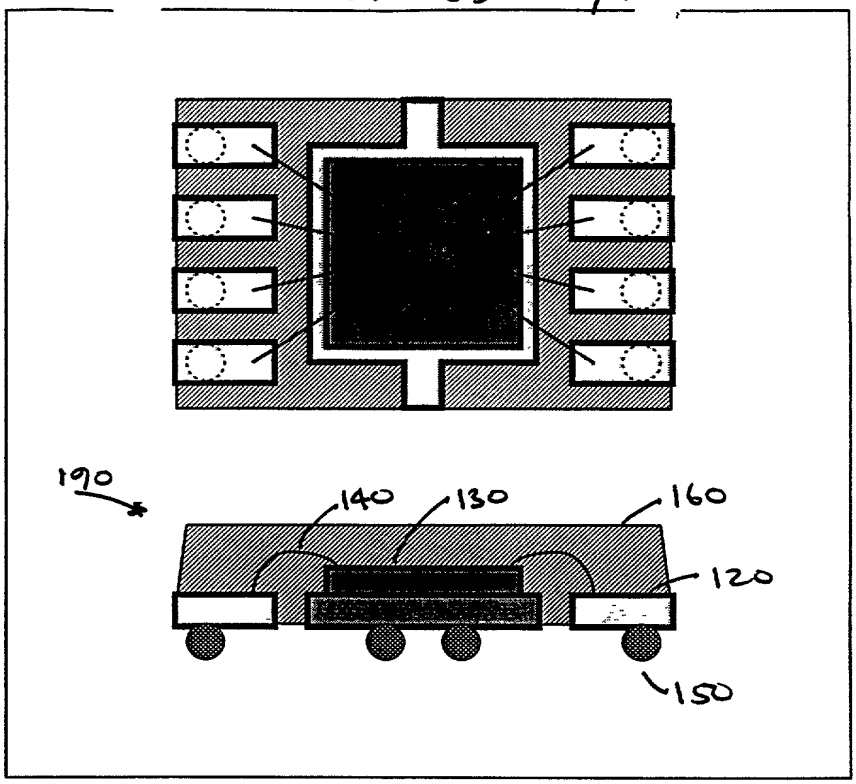

Fig. 1c: Finished BGA IC Package

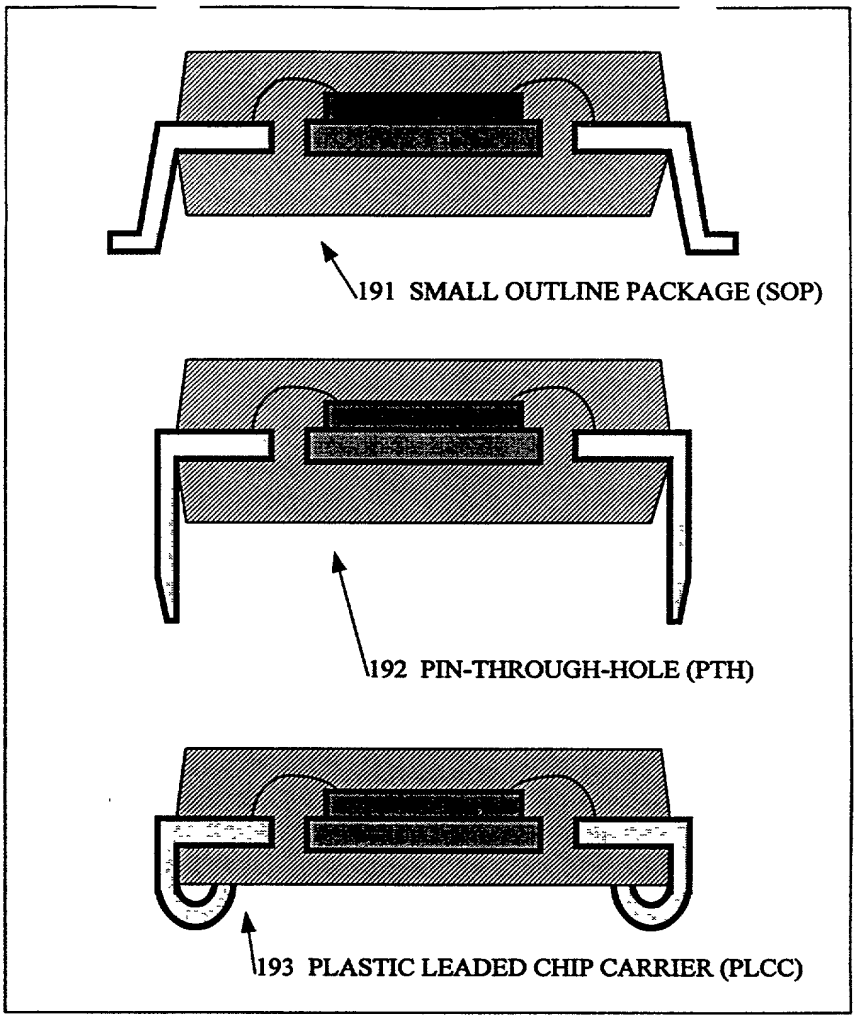

Fig. 1d: Examples of IC Packages

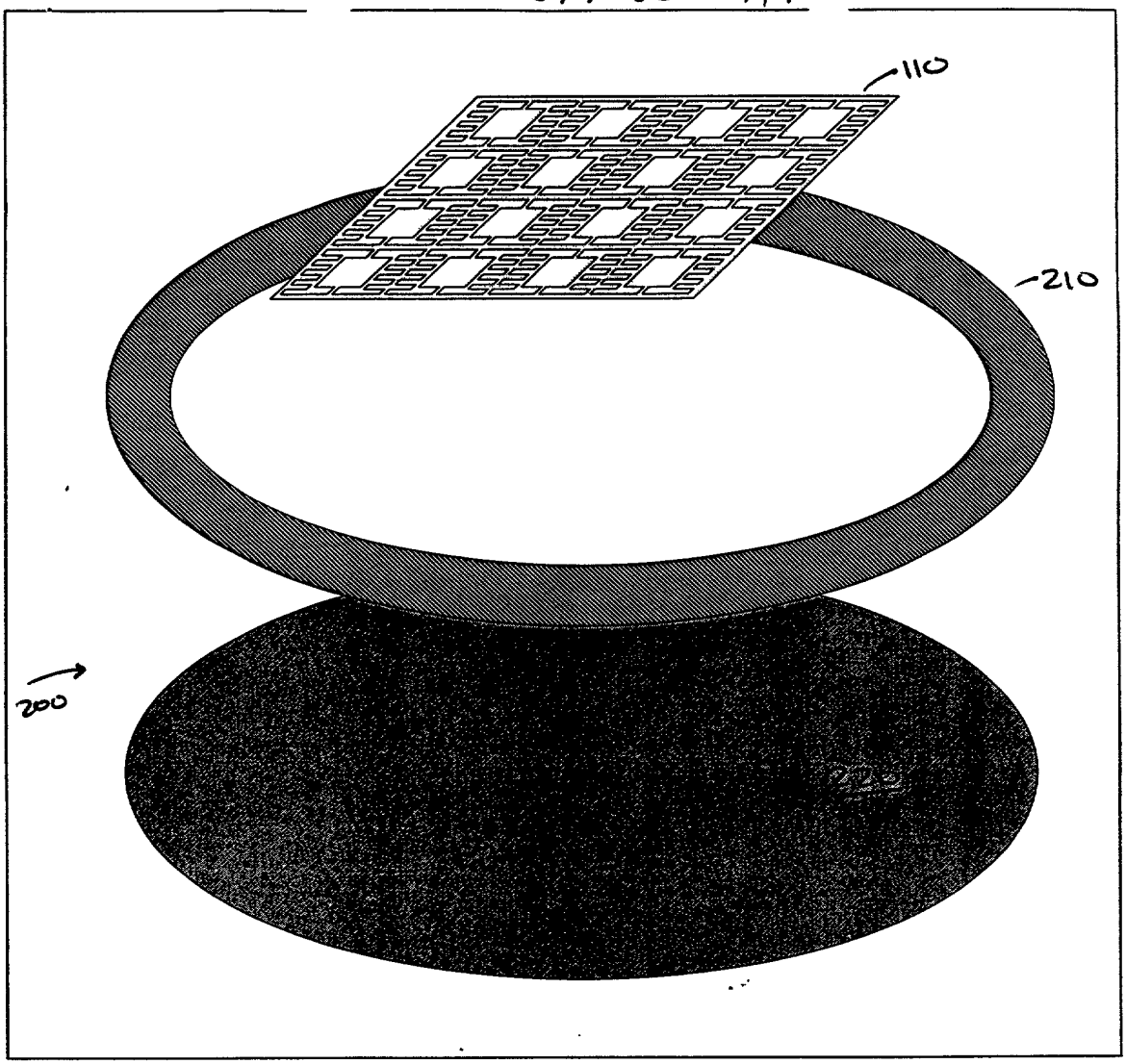

Fig. 2a: Lead Frame Panel Support Structure

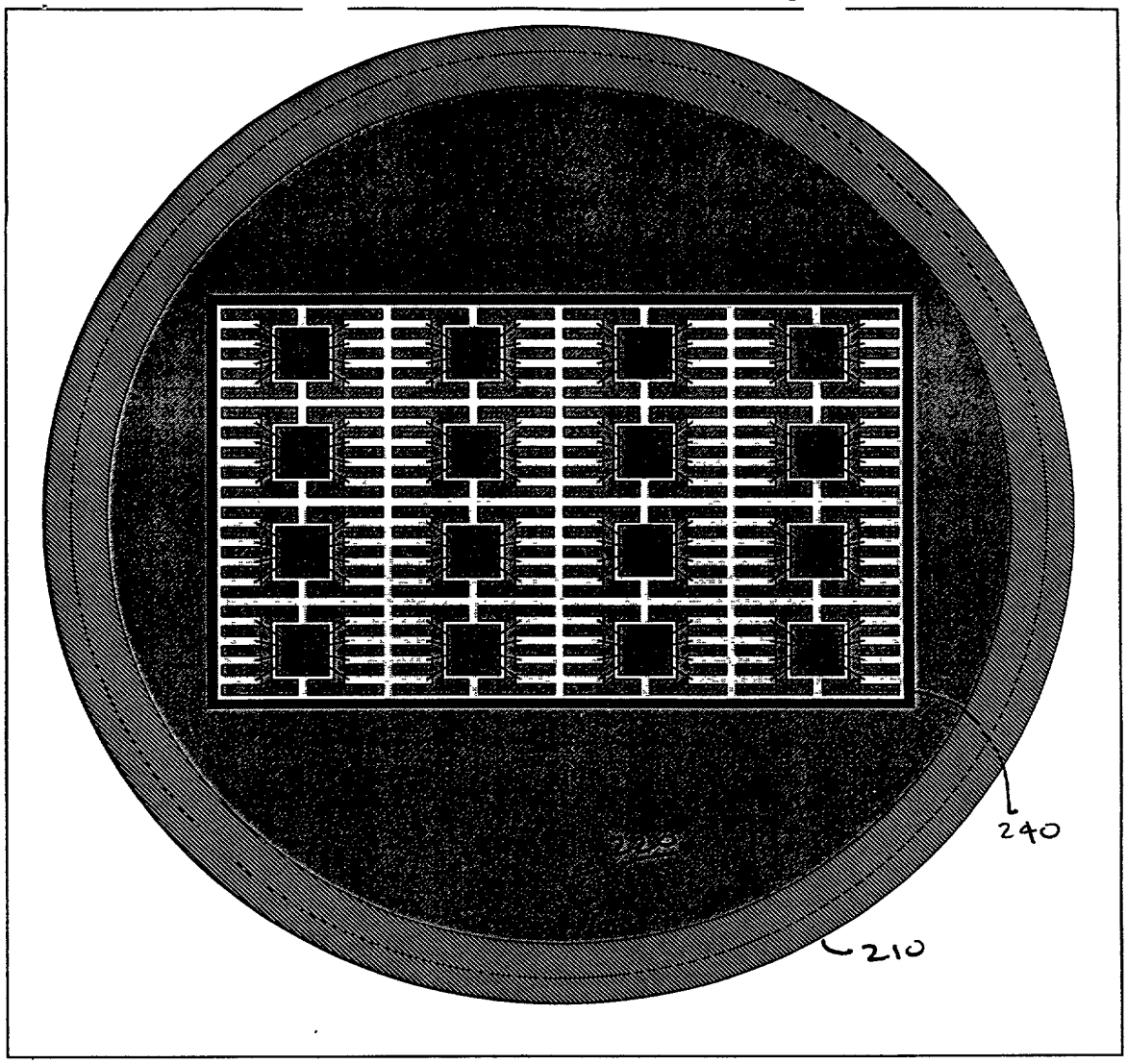

Fig. 2b: Lead Frame Panel Mounted on Support Structure with IC Chips Installed

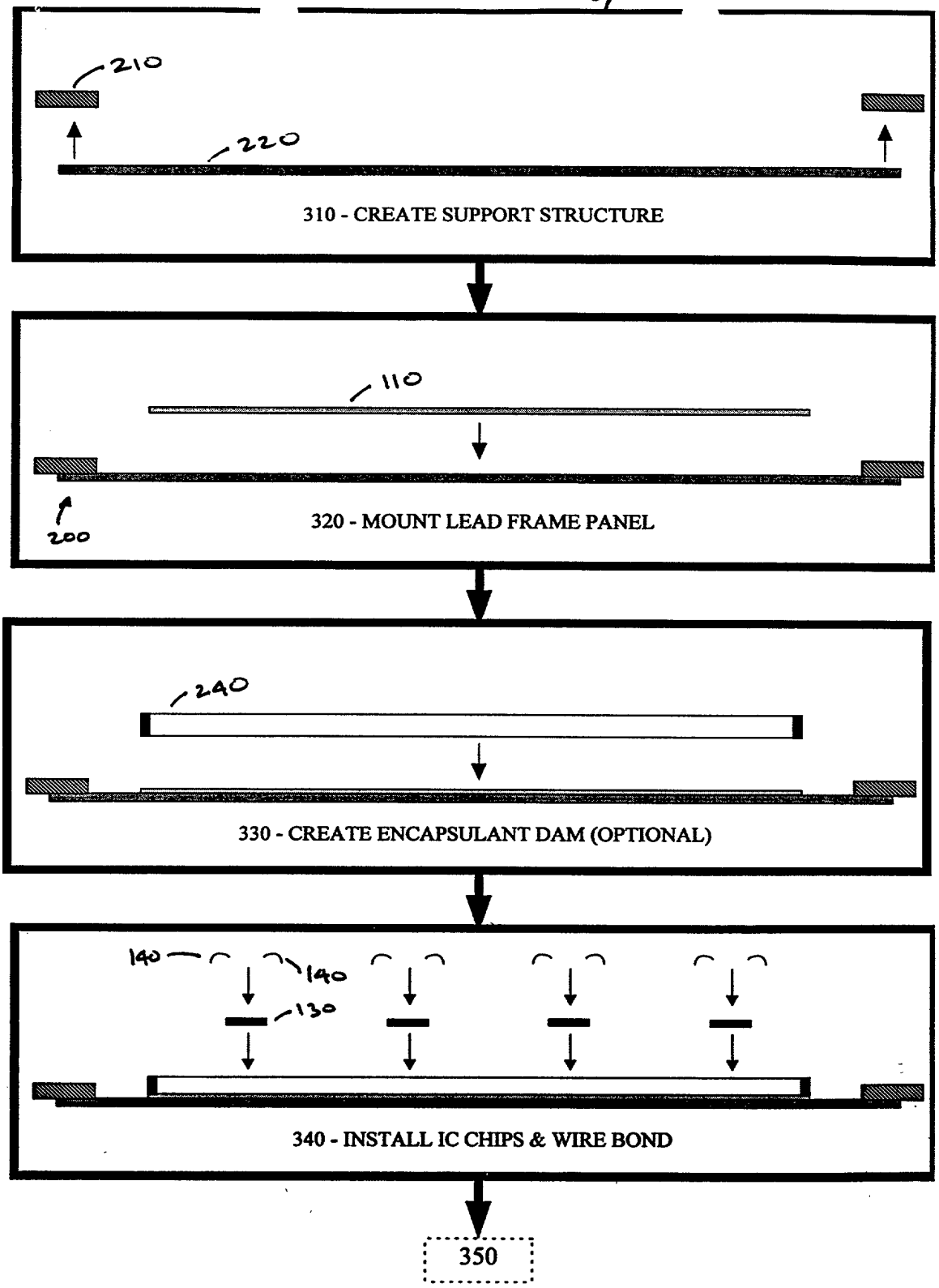

Fig. 3a: Flow Chart for Lead Frame BGA Process Using an Embodiment of the Present Invention, Part 1

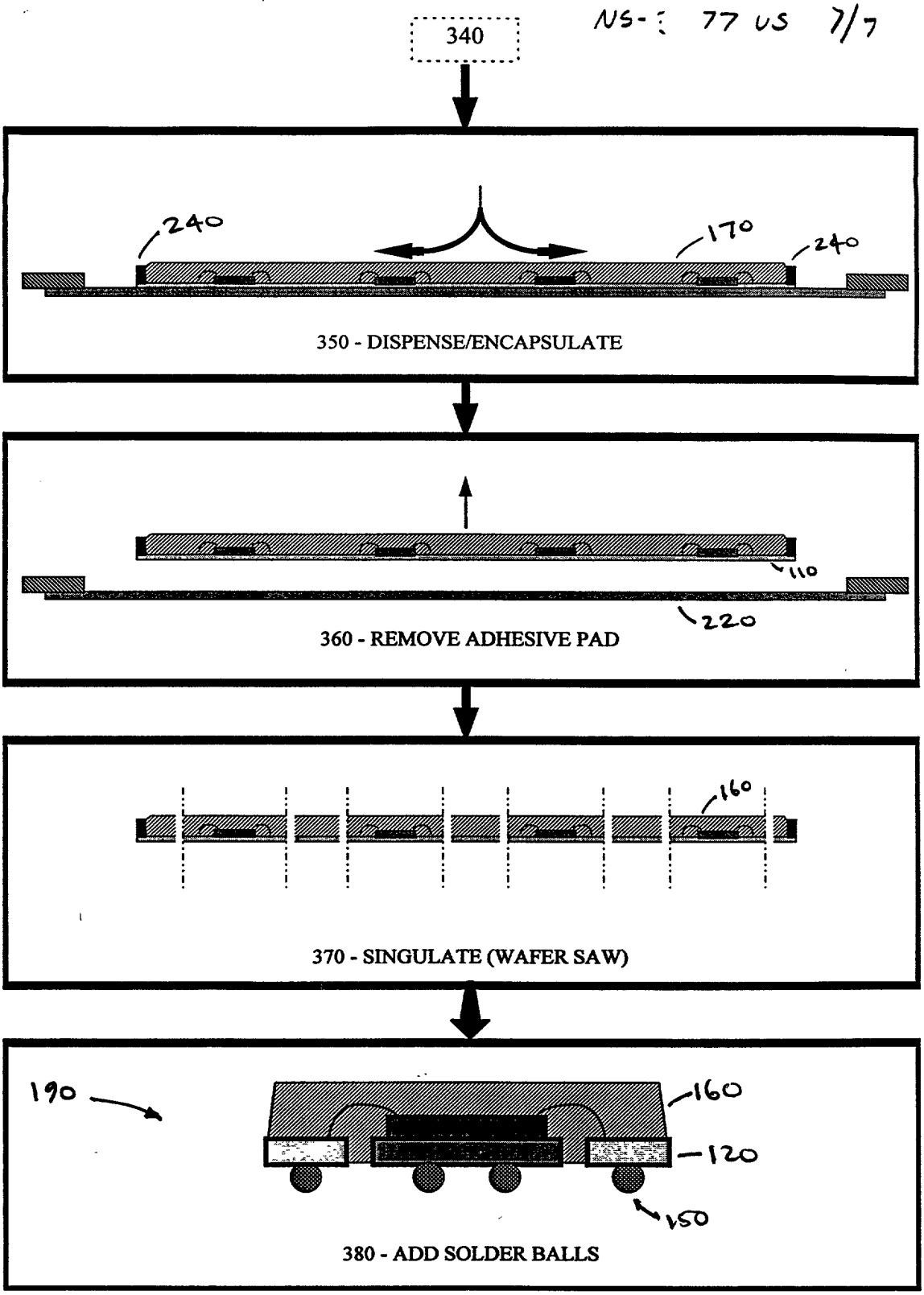

Fig. 3b: Flow Chart for Lead Frame BGA Process Using an Embodiment of the Present Invention, Part 2

DECLARATION FOR PATENT APPLICATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below adjacent to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of subject matter (process, machine, manufacture, or composition of matter, or an improvement thereof) which is claimed and for which a patent is sought by way of the application entitled Lead Frame Chip Scale Package

which (check) ☒ is attached hereto.
☐ and is amended by the Preliminary Amendment attached hereto.
☐ was filed on _____ as Application Serial No. _____
☐ and was amended on ___ (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information, which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, § 119(a)-(d) of any foreign application(s) for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America listed below and have also identified below any foreign application(s) for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America filed by me on the same subject matter having a filing date before that of the application(s) of which priority is claimed:

Prior Foreign Application(s)			Priority Claimed	
Number	Country	Day/Month/Year Filed	Yes	No
N/A			☐	☐

I hereby claim the benefit under Title 35, United States Code, § 119(e) of any United States provisional application(s) listed below:

Provisional Application Number	Filing Date
N/A	

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) or PCT international application(s) designating the United States of America listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior application(s) in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose information, which is material to patentability as defined in Title 37, Code of Federal

Regulations, § 1.56, which became available between the filing date of the prior application(s) and the national or PCT international filing date of this application:

Application Serial No.	Filing Date	Status (patented, pending, abandoned)
N/A		

I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and to transact all business in the United States Patent and Trademark Office connected therewith:

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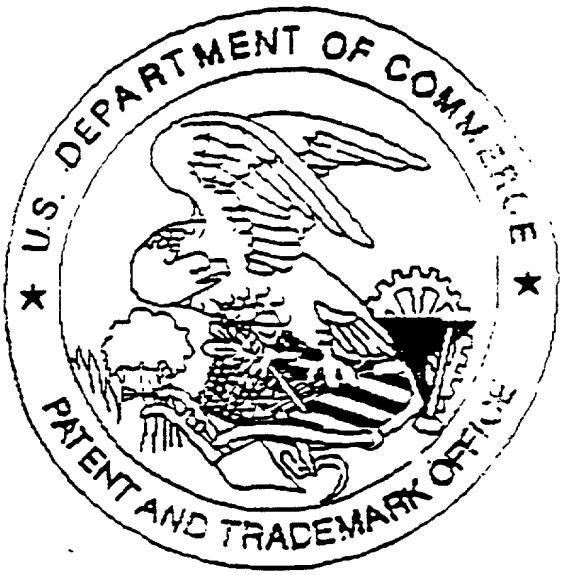

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